## REMARKS

Claims 1-10, 33-35, 46-50 were presented for examination. Claims 10 and 47 have been canceled without prejudice, and Claims 1-9, 33-35, 46, and 48-50 have been amended. Accordingly, Claims 1-9, 33-35, 46, and 48-50 are presently pending before the Examiner. Further examination and reconsideration are respectfully requested in view of the amendments and remarks made in this Response.

The Examiner required that a new title, clearly indicative of the claimed invention, be supplied. Accordingly, the title has been amended to clearly indicate the invention to which the claims are directed.

The Examiner indicated that the current status of the cross-referenced patent applications should be added to the specification. Accordingly, the specification has been amended to indicate the current status of the cross-referenced patent applications.

Claims 5 and 8 were objected to owing to a lack of clarity. Claims 5 and 8 have been amended to clearly indicate the claimed subject matter.

Claims 1-10, 33-35, 46-50 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Johnson *et al.* (U.S. Patent 4,581,990; hereinafter "Johnson") in view of Manning (U.S. Patent 5,652,724; hereinafter "Manning") or Olsen *et al.* (U.S. Patent 4,519,028; hereinafter "Olsen"). Claims 10 and 47 have been canceled without prejudice, and thus the rejection with respect to those Claims is moot.

Applicants respectfully disagree with the Examiner's contention that Johnson "indicates" an asynchronous memory interface. In view of Applicants position on Johnson, Applicants contend that the combination of Johnson, and Manning or Olsen is inoperative. Applicants further contend that the combination of Johnson, and Manning or Olsen is improper, and that the claims, as amended, are non-obvious in view of Johnson, and Manning or Olsen.

Johnson

Johnson discloses a RISC processor 101 connected to a data store 103 via shared address bus 111 and data bus 120. (*See*, Johnson, FIG. 1.) The "interface," provided by three separate buses (*see*, Johnson, col.2, lines 38-46), is synchronous (*see*, Johnson, col.8, lines 28-31). In Johnson, both burst and pipelined instructions are provided to access a memory. (*See*, Johnson, col. 10, lines 48-65.)

It is the Examiner's contention that the col. 10, lines 50-54, in Johnson indicates asynchronous memory operation. In portion of Johnson cited by the Examiner, the Examiner apparently relies on use of *IRDY or *DRDY signals for a "simple access" as justification for disclosing asynchronous memory operation.

In Johnson, a timing diagram is provided for each of the following types of memory access: "instruction read - simple access" (*see,* Johnson, FIG. 4), "instruction read - pipelined access" (*see,* Johnson, FIG. 5), and "instruction read - establishing burst mode access" (*see,* Johnson, FIG. 6). In each timing diagram in Johnson, a system clock signal ("SYS CLK" or "SYSCLK") is shown along with the *IRDY signal, and the *IRDY signal is synchronized to the SYSCLK signal. Johnson defines the *IRDY signal as an instruction ready signal to a processor to indicate that a valid instruction is on instruction bus 115. (*See,* Johnson, col.6, lines 22-25.) Accordingly, the *IRDY signal is provided to a processor in a synchronous manner with respect to the SYSCLK signal.

Johnson defines the *DRDY signal as a data ready signal to a processor indicating valid data is on data bus 120 for loads (*i.e.*, a completed read) and indicating an access is complete for stores (*i.e.*, data need not be driven on data bus 120 any longer). (*See,* Johnson, col.7, lines 22-27.) The *DRDY signal only indicates that an access is complete, not that the information is accessed in a synchronous or asynchronous manner.

In sum, the *IRDY signal is described with reference to SYSCLK, and the *DRDY signal provides no insight as to whether an access is synchronous or asynchronous. Thus, it is respectfully submitted that Johnson does not suggest or "disclose asynchronous operation" as asserted by the Examiner, rather it discloses a synchronous interface with a burst or pipelined mode command inquiry to a "data store 103."

Manning

Manning describes switching between burst EDO and standard EDO modes of operation (*see,* Manning, col. 6, lines 14-16), and describes switching between standard fast page mode and burst mode (*see,* Manning, col. 6, lines 14-16). In Manning, a mode register 40 is provided for this switching (*see,* Manning, FIG. 1). In Manning, this mode switching is described in the context of an asynchronously-accessible memory. Manning does not describe or suggest a pipelined mode. — see col 5 line 40-50

Applicants position is that the systems of Johnson and Manning are so different that there is no suggestion to combine them. The asynchronously-accessible memory of Manning with standard fast page mode or burst mode circuitry is a distinctly different system than the synchronous memory interface of Johnson with pipelined or burst mode instructions. Accordingly, there is no suggestion to combine Johnson and Manning.

Olsen

Olsen shows a CPU 10 with an operating mode register 72. (*See*, Olsen, FIG. 2.) Olsen discloses an asynchronously generated column address signal and an asynchronously generated priority-in (PI) signal in response to a row address signal (RAS) (*see*, Olsen, FIGS. 6 to 13). The RAS, CAS, and PI signals are provided to a memory controller 20 for accessing memory units 11 (*see*, Olsen, FIGS. 1 to 2). Accordingly, Olsen discloses and shows accessing a memory in an asynchronous manner. Notably, Olsen does not disclose or show a pipelined mode of operation.

Applicants position is that the systems of Johnson and Olsen are so different that there is no suggestion to combine them. The asynchronously accessible memory of Olsen is distinctly different from the synchronous interface of Johnson. Accordingly, there is no suggestion to combine Johnson and Olsen.

Improper Combination

The Examiner is contending that by placing the mode register of the memory of Manning or the mode register of the CPU of Olsen into block 103 labeled data store 103 of Johnson, the claimed invention is obvious. Applicants respectfully traverse this rejection. In FIG. 3A of Johnson, a processor inquires of a slave device, such as a memory, whether "pipeline or burst" mode is supported. Therefore, there is nothing in Johnson that describes how to support both pipelined and burst mode access in a memory. As Johnson provides no description of a memory having both pipelined and burst mode access, there is no proper basis for adding to it the mode register of Manning or Olsen. Therefore, it is Applicants position that the combination of Johnson with Manning or Olsen is improper hindsight reconstruction in view of the present invention, and accordingly respectfully requests the Examiner to withdraw the rejection.

Claims 1-9, 33-35, 46, and 48-50, As Amended

In contrast to Johnson which discloses a synchronous interface for operating a "data store", all the pending independent claims, as amended, recite an asynchronously-accessible storage device, an asynchronously-accessible memory device, or an asynchronous DRAM. In contrast to Johnson, Manning and Olsen, the present invention provides a memory having both pipelined and burst modes of operation.

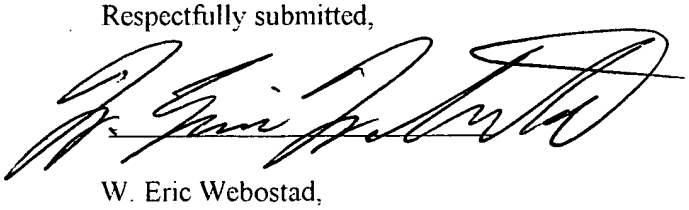
It is therefore respectfully submitted that the combination of the synchronously interfaced "data store" of Johnson with the mode circuitry of Manning or Olsen does not render obvious the present invention as claimed. Accordingly, it is respectfully submitted that Claims 1, 33, 46, and 50 are allowable over the art of record. Claims 2-9, 34-35, and 48-49 are dependent on an allowable base claim, and thus are likewise allowable.

Conclusion

It has been shown that Johnson discloses a synchronous, not an asynchronous, interface to a memory, and accordingly, the combination of Johnson, and Manning or Olsen has been shown to be inoperative and improper. Claims 1-9, 33-35, 46, and 48-50, as amended, have been shown to distinguish over the applied references of Johnson, and Manning or Olsen.

For the above-reasons, it is believed that Claims 1-9, 33-35, 46, and 48-50, all the pending claims, are allowable. As it is believed that the application is in condition for allowance, such allowance is earnestly solicited.

Respectfully submitted,



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